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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/694,450 | 10/27/2003 | Benyong Zhang | P05719 | 8900 |

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| EXAMINER | |
|---|---|
| NGUYEN, MINH T | |
| **ART UNIT** | **PAPER NUMBER** |
| 2816 | |

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/694,450 | ZHANG, BENYONG | |
| | Examiner | Art Unit | |
| | Minh Nguyen | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-10,12-17 and 20* is/are rejected.

7)☒ Claim(s) *6,11,18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/5/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

1. The disclosure is objected to because of the following informalities: the summary of invention section and its header are missing. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 7, 10 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 7, the predetermined amount recited on line 1 lacks antecedent basis. The N and X variables recited on line 2 are undefined.

As per claims 10 and 17, the same problems exist as discussed in claim 7 regarding the recited N and X variables.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,570,457, issued to Fischer.

Fischer discloses a method (figure 1) for providing a phase-locked loop with reduced spurious tones, comprising:

comparing a reference clock signal (FREF) to an internal clock signal (the signal from the divider 16) to generate a first signal (the signal from the phase detector 18);

sampling the first signal (use the sample and hold circuit 22) based on a sampling clock signal (the sampling clock signal on line 20) to generate a second signal (the sampled signal), the sampling clock signal reduced with respect to the reference clock signal (the frequency is reduced by the divider 21); and

generating the internal clock signal based on the second signal (use the controlled oscillator 14 and the divider 16).

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-5, 7-10, 12-17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,570,457, issued to Fischer in view of US Patent No. 5,920,233, issued to Denny.

As per claim 15, Fischer discloses a phase-locked loop (figure 1), comprising:

a spur reduction circuit (the frequency divider 21) operable to receive a reference clock signal (FREF) and to divide the reference clock signal by a predetermined value, D, to generate a reduced frequency signal (this is merely the function of a frequency divider, i.e., dividing a frequency of a clock signal by a predetermined number, column 2, lines 34-45);

a phase detector (phase detector 18) operable to compare the reference clock signal to an internal clock signal to generate a difference signal indicating the phase difference between the reference signal and the internal clock signal (this is a function of any phase detector in a PLL);

a stabilization filter (the filter 19) coupled to the phase detector (16), the stabilization filter operable to generate a stabilized signal (at the output of the filter 19);

a sampling circuit (sample and hold circuit 22) coupled to the stabilization filter (19) and to the spur reduction circuit (21), the sampling circuit operable to sample the stabilized signal based on the sampling clock signal to generate a sampled output signal (this is merely a function of a sample and hold circuit);

an oscillator (the controlled oscillator 14) coupled the sampling circuit, the oscillator operable to generate an output frequency signal (the output signal) based on the sampled output signal; and

a feedback divider (the feedback frequency divider 16) coupled between the oscillator and the phase detector, the feedback divider operable to divide the output by a predetermined

amount to generate the internal clock signal (the signal from the frequency divider 16 to the phase detector 18).

Fischer does not explicitly disclose a clock/buffer circuit coupled the spur reduction circuit and a charge pump coupled to the phase detector as called for in the claim.

Regarding the recited clock/buffer circuit limitation, the examiner takes Official Notice the fact that it is well-known in the art that when interfacing two circuit blocks which are not compatible, a buffer is inserted in between so that the two circuit blocks can be functioned properly together.

It would have been obvious to one skilled in the art at the time of the invention was made to insert a clock/buffer circuit coupled between the spur reduction circuit 21 and the sampling circuit 22 in the Fischer's PLL. The motivation and/or suggestion is to ensure the spur reduction circuit 21 and the sampling circuit 22 would be able to function together.

Regarding the recited charge pump limitation, Denny explicitly discloses a PLL circuit (figure 2) which includes a charge pump (108) between a phase detector (106) and the filter (110), and further, he clearly indicates (figure 1) that it is well-known in the art that the charge pump is merely an optional circuit in a PLL circuit. As clearly shown in figure 2 of Denny, the charge pump 108 functions merely to convert the phase difference indication from the phase detector to a different form of signal that is suitable for the VCO.

It would have been obvious to one skilled in the art at the time of the invention was made to include a charge pump between the phase detector and the filter in the Fischer's PLL circuit. The motivation and/or suggestion would be to ensure the phase difference indication from the phase detector has a proper form for use in the downstream circuits.

As per claim 16, the combination discussed herein above does not disclose an input divider to reduce the frequency of the reference clock signal as called for in the claim.

The examiner takes Official Notice the fact that including a divider to reduce the frequency of a reference clock signal in a PLL circuit is a well-known practice. The purpose of the practice is to ensure the PLL circuit to operate reliable when the reference input frequency is high and components used to implement the PLL circuit could not function reliable with such a high frequency.

It would have been obvious to one skilled in the art at the time of the invention was made to include an input divider to reduce the frequency of the reference clock signal in the Fischer's PLL circuit. The motivation and/or suggestion would be to ensure the Fischer's PLL circuit to be able to function in applications which require the PLL to receive a very high input frequency clock signal.

As per claim 17, the combination discussed herein above does not disclose specific values for N, X, D and R as called for in the claim.

However, as held by the court, when the general condition is met, the act of varying the parameters in a circuit is not patentable. In this instant case, the structure of the PLL is disclosed as discussed in claim 16, changing the divider values are not patentable since the practice can be done by an average person skilled in the art.

It would have been obvious to one skilled in the art at the time of the invention was made to set the values of N, X, D and R to specific values recited in the claim. The motivation and/or suggestion would be to comply with the requirement in a specific application.

As per claim 20, the recited lowpass filter reads on the loop filter 12.

As per claim 8, this claim is merely a method to operate the PLL discussed in claim 1. Since the PLL discussed in claim 1 has the recited structure, the method to operate such a PLL is seen as obvious.

As per claims 9-10, these claims are rejected for the reasons noted in claims 16-17, respectively.

As per claims 12-13, figure 2 of Denny clearly shows the recited limitations.

As per claim 14, this claim is rejected for the reason noted in claim 20.

As per claims 2, this claim is rejected for the reason noted in claim 8.

As per claim 3, this claim is rejected for the reasons noted in claim 12 and 13.

As per claims 4-5 and 7, these claims are rejected for the reasons noted in claims 14, 10 and 10, respectively.

### *Allowable Subject Matter*

5. Claims 6, 11 and 18-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 18-19 are allowable because the prior art of record fails to disclose or suggest the inclusion of a clock/buffer circuit which buffering the clock signal and the inverted clock signal by performing the function recited in claim 18.

Claims 6 and 11 are allowable for the same reason noted in claim 18.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

4/29/05

Minh Nguyen
Primary Examiner
Art Unit 2816